Final Project Report

High Power Gallium Nitride Devices for Microwave and RF Control Applications

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submitted to Program Monitor

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14. ABSTRACT
Gallium Nitride devices were studied for use in microwave and RF control applications, primarily as electronic switch elements. For the test devices studied, broadband switch cutoff frequencies in excess of 130 GHz were seen, with cutoff frequencies as high as 400 GHz possible with the next generation devices. Second order distortion intercept points of greater than 50 dBm should be achievable with current gallium nitride technologies.

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Executive Summary

This project focused on the small and large signal behavior of gallium nitride (GaN) FETs in high power microwave control applications. A small signal linear equivalent circuit model was developed that shows good agreement with experimental data taken on GaN HFETs provided to Villanova University by Les Eastman of Cornell University. For 0.25 micron gate length AlGaN/GaN devices with 2DEG sheet resistances of 1900Ω/sq, the microwave on-state resistance is approximately 2.6 Ohm-mm at +1.5 volts gate bias. For 500 Ω/sq sheet resistances, the microwave on-state switching resistance is anticipated to be approximately 1.0 Ohm-mm at the same bias level. With the improved sheet resistance wafers, viable microwave and RF switching devices that compare favorably with current GaAs switch technology in terms of switch insertion loss and isolation can be made with 250 micron gate peripheries. Off-state switch capacitances of 400 fF/mm are achievable at -3.0 volts gate bias for source-drain spacings of 2.0 microns. The off-state capacitances are shown to not be a function of gate length. For the 500 Ω/sq (1900 Ω/sq) devices, broadband switch cutoff frequencies in excess of 400 GHz (130 GHz) are easily achievable.

A physical model describing the origin of the distortion in microwave and RF switches using AlGaN/GaN HFETs indicates that the field-dependent mobility in the channel two dimensional electron gas is the dominant mechanism in generating distortion in these devices. The model indicates HFET turn-off voltages in the range of -1.0 to -1.5 volts provide the lowest distortion in series switch configurations using AlGaN/GaN HFET devices. The intercept point can be increased (distortion reduced) by decreasing the channel resistance of the HFET. A comparison of the HFET switch with MESFET switches shows that the HFET switch generates more distortion than its MESFET counterpart. In addition, the frequency response of HFET switches is the opposite of the MESFET switch, with less distortion at low frequencies. The distortion is found to be nearly constant with frequency. Second order distortion intercept points in the range of 50 to 60 dBm should be achievable with current AlGaN/GaN technology.

Under high power operation it was found that the on-state resistance was a function of the applied microwave power. This resistance changed up to 20% over the range of –5 to 20 dBm applied microwave power with shunt connected devices. This phenomenon showed a weak frequency dependence. Modeling efforts appear to verify this increase in resistance over the range of powers tested. This effect may limit the use of these devices for very high power operation

Project Outcomes: List of Publications Arising From This ONR Funding

1. "On-state Distortion in High Electron Mobility Transistor Microwave and RF Switch Control Circuits", Robert H. Caverly and Kennith J. Heissler, *IEEE Transactions on Microwave Theory and Techniques*, January, 2000.
2. "GaN-Based Microwave and RF High Power Control Circuits", *IEEE Transactions on Microwave Theory and Techniques,* with N. Dorozdovski, in revision.
3. "GaN Based Microwave and RF High Power Switches", presentation at *1999 1st Gallium Nitride Electronic Device Workshop, Cornell University.*
4. "GaN Based High Electron Mobility Transistors for Microwave and RF Control Applications", *1999 International Microwave and Optoelectronics Conference IMOC'99*, with N. Dorozdovski.
5. "AlGaN/GaN Material Properties and HFET Shunt Switch RF Performance", *1999 International Conference on Solid State Devices and Materials SSDM-99*, with N. Dorzdovski.

Brief Statement of Technology Advancement from Original Proposal

The 15 month effort completed **Phase 1, Task A**, as defined in the proposal originally submitted to the Office of Naval Research. This task, *Develop a linear model for GaN-based devices as a microwave and RF control element,* is discussed in detail in this report and shows good agreement with experimental data performed on experimental AlGaN/GaN devices obtained from Lester Eastman's research group at Cornell University. An initial approach for **Phase 1, Task B**, *Develop a nonlinear model to predict harmonic and intermodulation distortion generated by these devices,* has been completed for the on-state switch with the results published. This on-state model was refined and used to predict large signal effects in AlGaN/GaN microwave and RF switching devices. **Phase 3, Task A**, *Validate, and modify if necessary, these models with actual devices currently being fabricated by other ONR funded programs,* was also done. The HFETs from Cornell that we measured exhibited 2DEG sheet resistances of 1900 Ω/sq. The **Phase 1, Task A**, effort is based on measurements of these devices.

Small Signal Modeling of the AlGaN/GaN HFET Microwave and RF Switch

General Modeling Principles

The simplified small-signal equivalent circuit for the GaN-based heterojunction field effect transistor (HFET) in a switch application (Fig.1) consists of a parallel resistance R_{sd} and capacitance C_{sd}. The values of these equivalent circuit parameters are determined by the semiconductor material properties, transistor geometry and DC gate control voltage. From the equivalent circuit, the on-state resistance of the switching FET R_{sd} can be written as:

$$R_{sd} = R_{ch} + R_s + R_d, \tag{1}$$

where, R_{ch} is the heterointerface (or channel) resistance, and R_S and R_d are the parasitic source and drain resistance, respectively. The contribution of R_s and R_d to the total on-state switch resistance R_{sd} is negligible compared with the channel reistance R_{ch}. Since the two dimensional electron gas (2DEG) governs the resistance in the conductive channel, the total channel resistance may be estimated as:

$$R_{ch} = \rho_S \times \frac{L_{ch}}{W}, \tag{2}$$

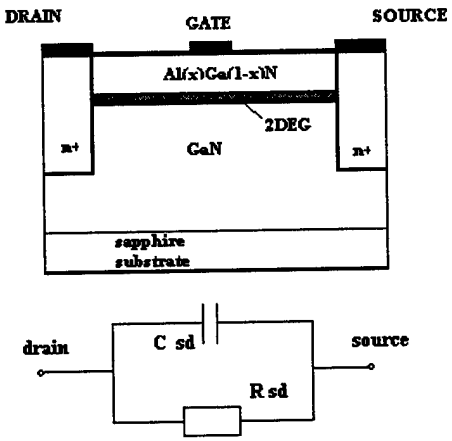

Figure 1. GaN HFET and its small-signal equivalent circuit.

where, ρ_S is the sheet resistance of $Al_XGa_{1-X}N$/GaN interface 2DEG, W is the gate width of HFET, and L_{ch} is the channel length (drain-source distance). The value of the sheet resistance is computed as:

$$\rho_s = \frac{1}{\mu_n n_s q}, \tag{3}$$

where q is the single charge, μ_n is the low-field mobility of 2DEG and n_s is the two-dimensional electron gas (2DEG) density which is the function of the DC control gate voltage and interface geometry. The full derivation for the channel resistance R_{ch} is in Appendix A.

The model for capacitance C_{sd} includes both voltage dependent and parasitic capacitances. The important parasitics are the source and drain metal coupling capacitance through air to the gate, the extrinsic capacitances that couple the source and drain above the semiconductor, and the intrinsic capacitances that couple through the GaN and substrate layers. The last three capacitances are present only in the off-state, when the 2DEG is suppressed by the gate voltage. These capacitances may be estimated using standard equations for MESFETs. The voltage dependent capacitances are presented by source-gate and drain-gate capacitances and capacitances between gate and inner side of the drain or source contacts. The full derivation for the capacitance C_{sd} is in Appendix B.

Measurements were performed on Cornell University GaN FETs to test the theoretical models on as-fabricated devices. Swept S-parameters measurements were performed on a variety of the devices over the frequency range of 2.5 to 7.0 GHz at a power level of 0 dBm, keeping the device in its so-called small signal regime. Figure 2 shows a typical computed and experimental DC control gate voltage characteristic of source-drain resistance at frequency of 2.5 GHz. The particular AlGaN/GaN FET chosen for this illustration exhibited a 150 micron gate width, a 0.3 micron gate length and a 2.0 micron source-drain spacing. The theory and experimental data show that, in the off-state R_{sd} (or R_{OFF}) is on the order of $k\Omega$, while in on-state R_{sd} (or R_{ON}) is about 30 Ohms, in good agreement. Source-drain capacitance C_{sd} does not exceed 100 femtofarades in both states as shown in Figure 3. Note also the agreement between both the measured and model resistance and capacitance curves. Appendix D contains typical values of simulation parameters. Similar results hold for other frequencies and devices tested.

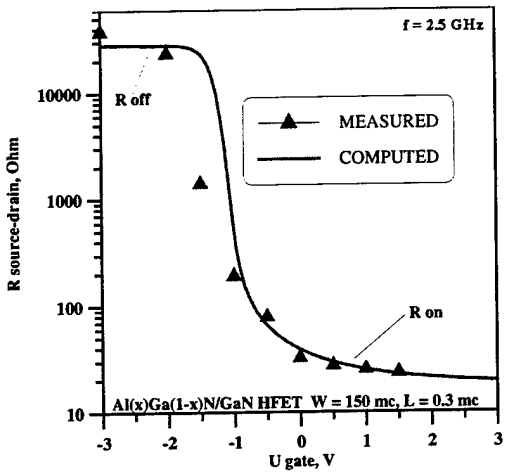

Figure 2. Measured On-State Drain-source switch resistance R_{sd} versus DC gate control voltage.

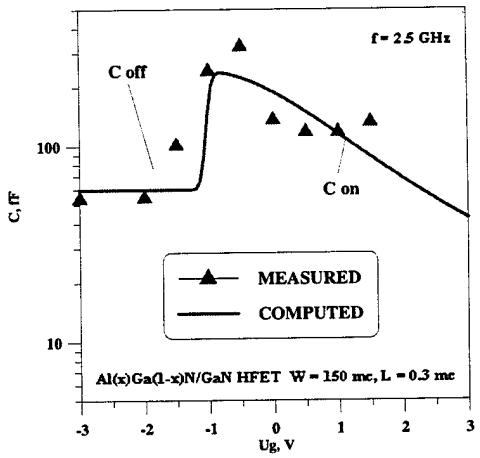

Figure 3. Measured Off-State Drain-source switch capacitance C_{sd} versus DC gate control voltage.

The model and experimental data indicate that both the resistance and capacitance vary rapidly in the vicinity of the threshold voltage, approximately -1.25 volts as shown in Figures 2 and 3. The lower value of capacitance for gate voltages below threshold is advantageous since lower insertion loss or isolation (depending on switch configuration) occurs with small capacitance values. The rapidly varying resistance in the voltage range of approximately zero volts to threshold indicates that the control device may also be used as a voltage variable resistance, a key factor for the development of variable microwave and RF attenuators. Of particular interest to designers of microwave and RF switch designers and fabricators is the relatively low resistance at zero volts gate bias. For control circuits using these devices, a unipolar power supply structure may be possible to effect the appropriate switching action. This requires a higher gate periphery than if +1.5 volts could be used, at the expense of increased off-state capacitance.

Figures 4 and 5 show simulations of on-state resistance R_{ON} and off-state capacitance C_{OFF} as functions of various parameters. R_{ON} is heavily dependent on 2DEG sheet resistance and ranges from 1.0 Ohm-mm to 2.9 Ohm-mm in 500 Ohm/sq and 1900 Ohm/sq devices, respectively, at 0.25 micron gate lengths. The figures also indicate that R_{ON} slightly decreases with increasing gate length when the gate voltage increases from 0.0 volts to +1.5 volts for both low and high 2DEG sheet resistance values.

This effect is due to the reduction of resistance directly under the gate while the source-gate and gate-drain resistances remain voltage-invariant. As the gate length increases, these parasitic resistances become smaller in value, for a given source-drain spacing, yielding the reduction in on-state resistance with increasing gate length. The off-state capacitance is seen to be constant for a given source-drain spacing over a range of gate lengths, with higher off-state capacitances for smaller source-drain spacings. The capacitance is relatively independent of 2DEG sheet resistance. The model indicates an off-state capacitance of 400 fF/mm for 2 micron source-drain spacing. A reduction in source-drain spacing increases the off-state capacitance but reduces the parasitic resistance in the on-state.

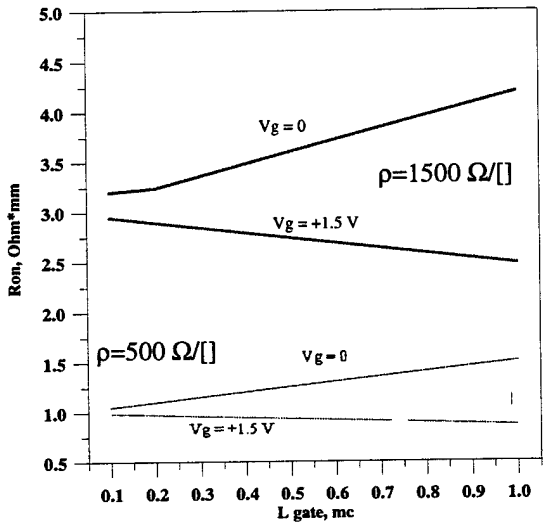

Figure 4. On-state resistance as a function of gate length using bias and sheet resistance as a parameter.

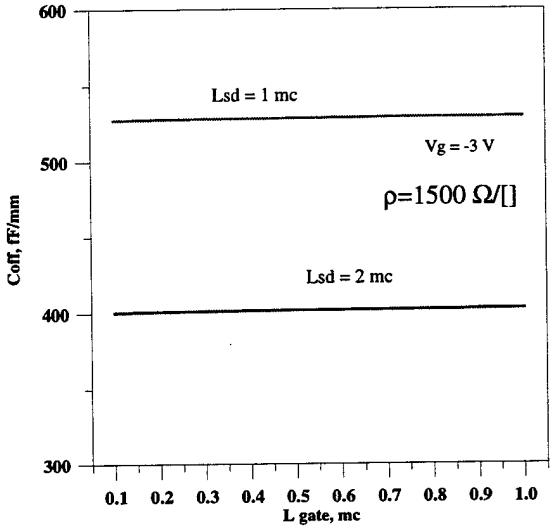

Figure 5. Off-state capacitance as a function of gate length using the source-drain spacing as a parameter.

Figures 6 and 7 show measured on-state resistance at zero and +1.5 volt gate bias as a function of gate length for 150 micron and 75 micron Cornell University AlGaN/GaN devices. For +1.5 volts gate bias, the model and measurements show an on-state resistance of approximately 3.5 Ohm-mm for 1900 Ohm/sq devices. Note the predicted slight decrease in R_{ON} at the higher gate bias voltage for larger gate length devices. Also shown in the figures is that the model underestimates the on-state resistance for smaller gate periphery. This may be due to measurement error.

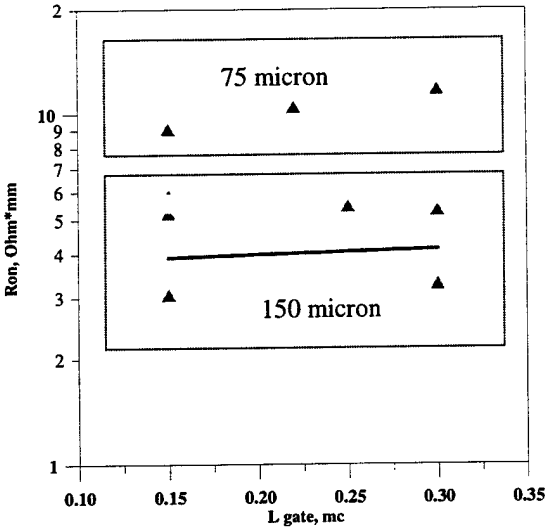

Figure 6. On-state resistance versus gate length for 0.0 volts gate bias.

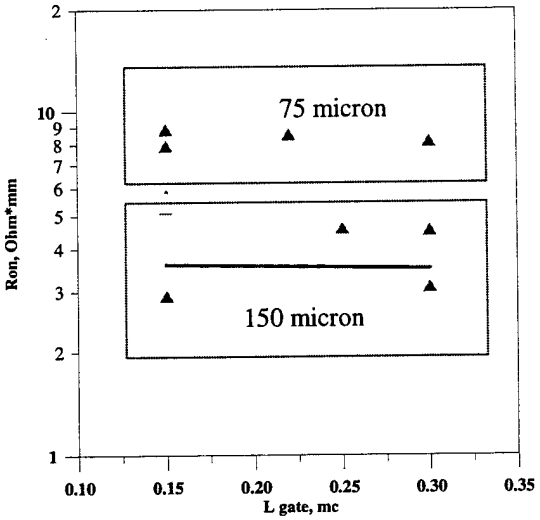

Figure 7. On-state resistance versus gate length +1.5 volts gate bias.

Figure 8 shows measurements of the off-state capacitance at -2.0 volts gate bias as a function of gate length for 75 micron and 150 micron gate periphery. With the exception of two outlying data points (more than likely due to measurement error), the model accurately predicts a constant off-state capacitance as a function of gate length at 380 fF/mm.

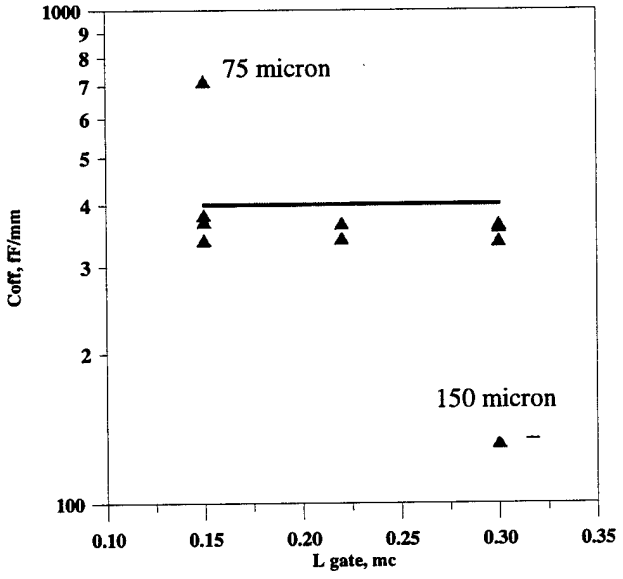

Figure 8. Off-state capacitance as a function of gate length at -2.0 volts gate bias.

The HFET on-state resistance R_{ON} and an off-state capacitance value, C_{OFF}, can be used to define

the broadband switch cutoff frequency:

$$f_C = \frac{1}{2\pi R_{ON} C_{OFF}}$$

This cutoff frequency can be used as a control circuit figure of merit in comparing different microwave and RF control technologies. Figure 9 shows f_C as a function of gate periphery W at different bias levels and device gate lengths for 2DEG sheet resistances of 1900 and 500 Ω/sq.

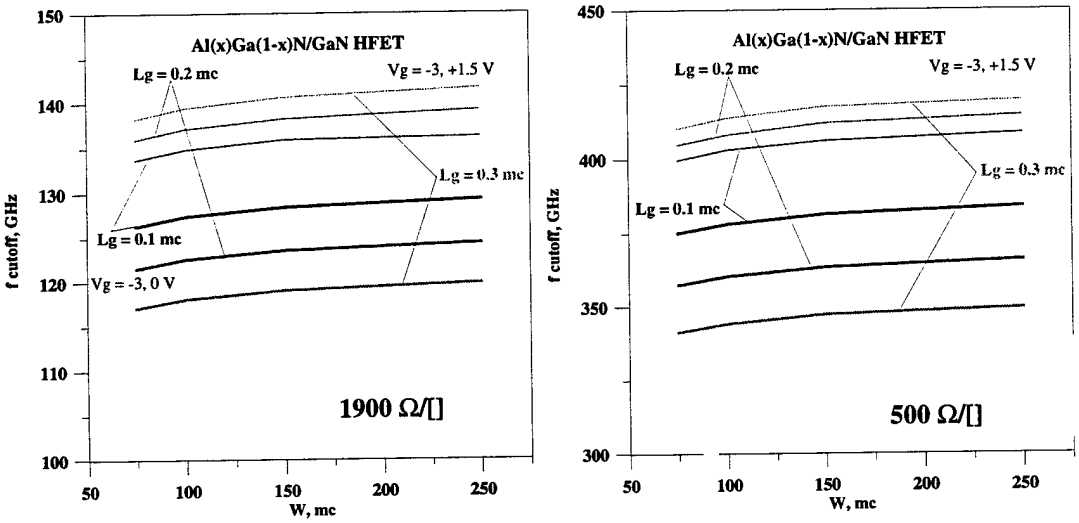

Figure 9. Switch cutoff frequency as a function of gate periphery W at different bias levels, device gate lengths and 2DEG sheet resistances.

The upper curves (dotted lines) show the cutoff frequency at +1.5 volts bias (minimum R_{ON}) and -3.0 volts bias (minimum C_{OFF}). The results show a weak dependence on both gate periphery and length, with broadband switch cutoff frequencies greater than 400 GHz for gate peripheries of 100 microns and larger for 500 Ω/sq sheet resistance devices.

Series and Shunt Microwave and RF Switch Characteristics

The main control FET parameters are on-state resistance R_{ON} (called R_{sd} for DC gate voltage above the threshold voltage) and off-state capacitance C_{OFF} (DC voltage is beyond the threshold voltage). These parameters determine the switch's RF impedance in the two switch states and therefore the two main RF switch parameters, insertion loss and isolation, are strongly dependent on them. In the

case of the shunt FET configuration, the isolation is determined by R_{ON}, while insertion loss by C_{OFF}. Multi-throw FET switches (for example, SPDT and nPmT) utilize a combination of series and shunt elements to improve insertion loss, isolation and linearity; therefore both device configurations (series and shunt) need to be studied for completeness. For the following discussion, single FET switch elements will be considered in a SPST switch configuration.

The two important switch parameters, insertion loss and isolation, may be written in the SPST shunt configuration as

$$IL = 10\log[1 + (0.5\omega C_{off} Z_0)^2] \text{ and } ISO = 20\log[1 + \frac{Z_0}{2R_{on}}] \quad (4)$$

whereas in the series SPST configuration, the two important switch parameters are given by:

$$IL = 20\log[1 + \frac{R_{on}}{2Z_0}] \text{ and } ISO = 10\log[1 + (\frac{1}{2\omega C_{off} Z_0})^2] \quad (5)$$

where both parameters are in terms of dB.

For switching or control GaN FETs, the value of the sheet resistance at the $Al_XGa_{1-X}N$/GaN 2DEG interface strongly influences the on-state resistance, therefore strongly affecting the shunt isolation or series insertion loss. Figures 10 and 11 illustrate this influence for series and shunt connected GaN FETs used as microwave and RF control elements. The curves show computed GaN HFET shunt and series connected switch losses versus DC gate voltage for different values of sheet resistance. For the shunt connected switch, there is little influence of the sheet resistance on the level of insertion loss, because they are determined by the C_{OFF}, but there is significant change in isolation as sheet resistance is changed. The converse in true in the series case; the isolation is high in the off state and independent of sheet resistance whereas the insertion loss is small for positive gate voltages.

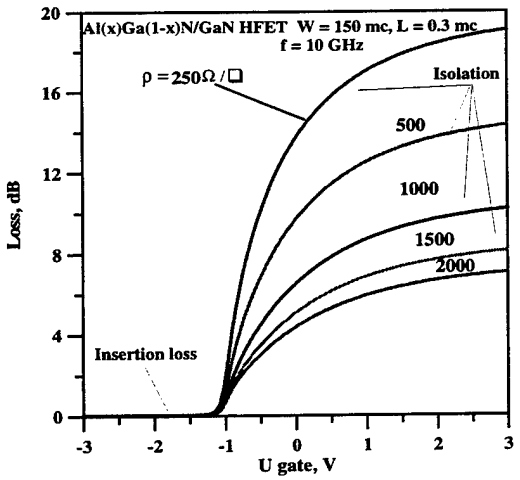

Figure 10. Shunt connected FET switch loss versus DC gate control voltage with sheet resistance as a parameter.

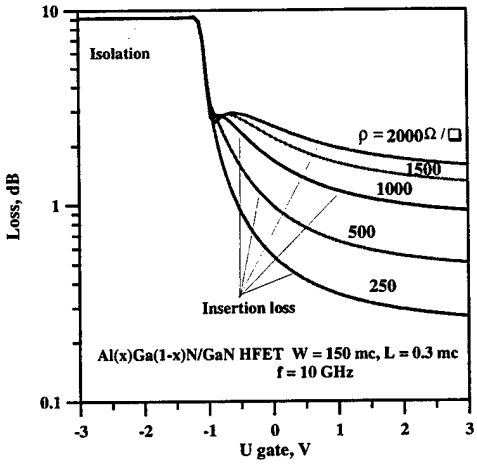

Figure 11. Series connected FET switch loss versus DC gate control voltage with sheet resistance as a parameter.

From Figure 11, a 500 Ω/sq. 2DEG will yield a series switch insertion loss of approximately 0.5 dB at 10 GHz for the switch geometry indicated, comparable with some current GaAs MESFET switch technologies. Further improvement in insertion loss can be obtained by increasing the gate width W of the GaN FETs; however, this will also increase the off-state capacitance and a subsequent degradation of series isolation. This effect is illustrated in more detail in Figures 12 and 13. In Figure 12, series connected GaN FET (W=150 microns, L=0.3 microns) insertion loss and isolation is plotted versus two different 2DEG sheet resistances, 1900 Ω/sq. and 450 Ω/sq.. These two sheet resistance values were chosen because they represent past and current fabrication technologies of the Cornell devices. By reducing the sheet resistance and thereby improving the 2DEG conducting properties, the insertion loss may be improved to 0.6 dB from 2.0 dB. The insertion loss is primarily determined by the on-state resistance and is constant up to 20 GHz. Since the capacitance is not a function of sheet resistance, the isolation is the same for the two devices and is approximately 10 dB at 10 GHz. Figure 13 shows additional improvement in insertion loss can be achieved by increasing the gate width from 150 to 250 microns. The insertion loss reduction is from 0.6 to 0.3 dB, comparable with current commercially available GaAs FET control devices. The increase in gate width, however, also increases the device capacitance with a corresponding decrease in isolation by approximately 2 dB.

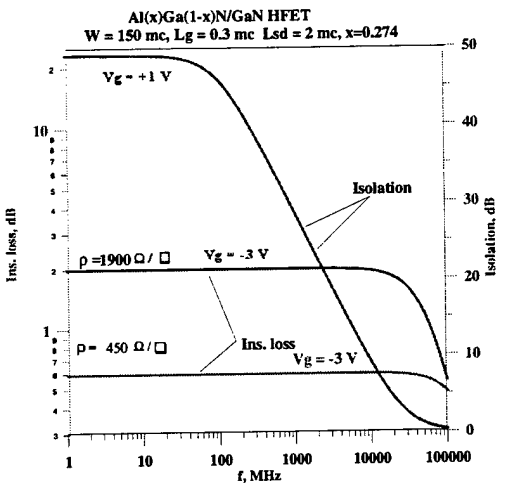

Figure 12. Series switch insertion loss and isolation for two different GaN sheet resistances as a function of frequency The gate length and width are 0.3 and 150 microns, respectively.

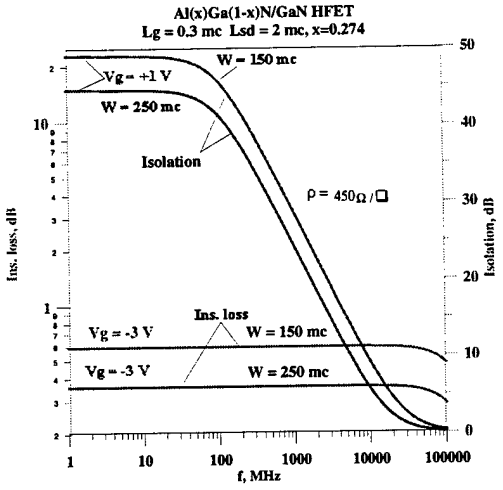

Figure 13. Series switch insertion loss and isolation for two different GaN gate widths as a function of frequency. The sheet resistance for the simulations is 450 Ω/sq.

Similar phenomenon occur for the GaN FET is shunt connected switch configurations. Figures 14 and 15 illustrate shunt switch isolation and insertion loss for different sheet resistances and gate widths. A reduction in sheet resistance (Figure 14) yields an improvement in switch isolation of approximately 4 dB with negligible effect on switch insertion loss. Increasing the gate width (Figure 15) yields a further 4 dB improvement in shunt switch isolation but at the expense of a slight increase in shunt insertion loss.

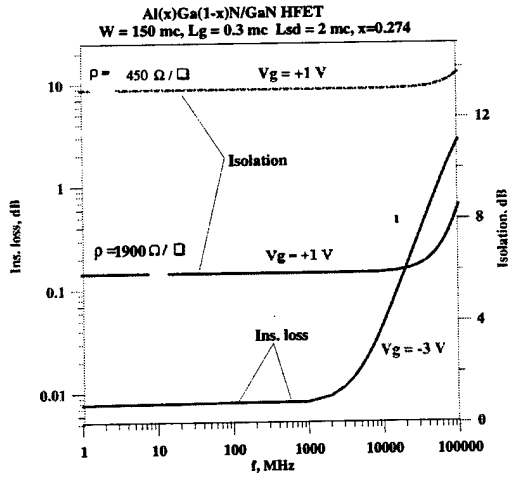

Figure 14. Shunt SPST switch insertion loss and isolation versus frequency with 2DEG sheet resistance as a parameter.

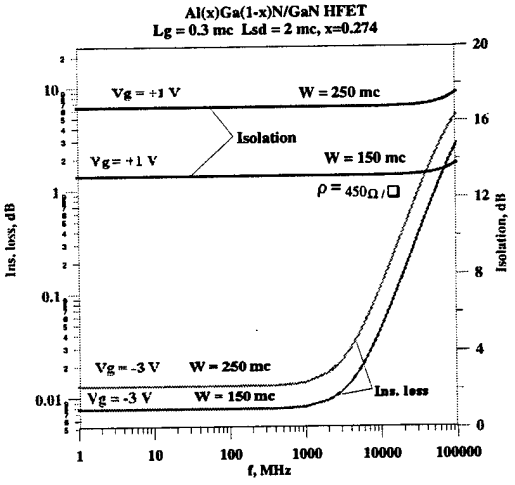

Figure 15. Shunt SPST switch insertion loss and isolation versus frequency with gate width W as a parameter.

Distortion Modeling of the AlGaN/GaN FET Microwave and RF Switch

Introduction

This section of the report presents the theoretical background describing the mechanism governing the nonlinearity in AlGaN/GaN high electron mobility transistor (HFET) switches. From the analytical study based on a model velocity-electric field profile in the AlGaN/GaN two dimensional electron gas, a method to predict the distortion products as a function of AlGaN/GaN HFET electrical parameters are presented. The current-voltage characteristics of the AlGaN/GaN HFET operating in the triode region are derived using a simple charge density and field-dependent mobility model. From these characteristics, load referenced distortion intercept points are derived. The theoretical discussion is found in Appendix C.

The combination of Equations C2 and C9 provide a means to compute the second and third order distortion intercept points for the GaN HFET switch. Using these equations, Figures 16 and 17 were produced, showing IP2 and IP3 as a function of the turn off voltage V_{off} for an AlGaN/GaN HFET at 1000 MHz and a zero gate voltage.

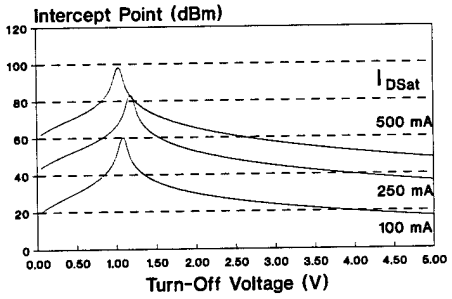

Figure 16. Second order distortion intercept point for the series connected GaN HFET microwave switch plotted versus GaN HFET turn-off voltage V_{Off} with the saturated drain current I_{DSat} as a parameter.

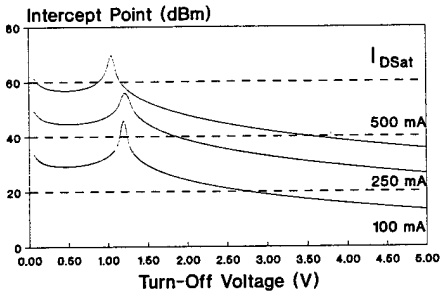

Figure 17. Third order distortion intercept point for the series connected GaN HFET microwave switch plotted versus GaN HFET turn-off voltage V_{Off} with the saturated drain current I_{DSat} as a parameter.

The drain saturation current I_{DSat} is used as a parameter for this illustration. The results indicate that GaN HFET turn-off voltages in the range -1.0 to -1.5 volts provide the highest levels of distortion intercept point (implying the lowest distortion) for a given drain current saturation parameter. The peak in the intercept point is caused by phase cancellation between the nonlinearity in the 2DEG mobility and the gate bias circuitry's dependence on V_{off}. The figures also show improvements in distortion intercept point at any turn-off voltage with increasing I_{DSat} that is due to the improved insertion loss (lower channel resistance) in these devices. The reduction in corresponding series resistance can be accomplished by increasing I_{DSat} through fabrication (by increasing the gate width W for example, at the expense of frequency response) or by a small positive gate voltage (V_{GS0}). Comparison with other HFET structures has indicated that the overall intercept point in the AlGaN/GaN technology is higher than its AlGaAs/GaAs HFET counterpart due to the higher saturation velocity and lower mobility in the AlGaN/GaN device.

The GaN HFET exhibits a slight frequency dependence in its distortion intercept point. Figure 18 shows the results of IP2 and IP3 simulations for an 0.25 micron gate GaN HFET with a saturated drain current of 250 mA, a turn-off voltage of -2.0 volts, values of C_{GS} and C_{GD} of 0.5 pF, and a gate bias resistance of 5 KΩ. The results indicate that the distortion intercept point is higher at low frequencies (less distortion) and changes to a somewhat lower value near the gate bias circuit cutoff frequency, approximately

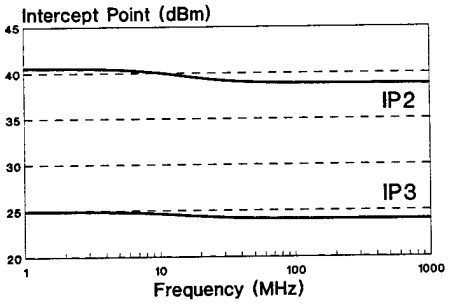

Figure 18. Second and third order distortion intercept point for GaN HFET as a function of frequency, showing a nearly constant level of distortion throughout the usable range of the HFET switch

$1/2\pi R_G(C_{DG}+C_{GS})$. The frequency dependence of the GaN HFET switch distortion is opposite of GaAs MESFET switch distortion where lower intercept points occur at low frequencies [22]. This phenomenon can be explained in the following way. In the GaN HFET, changes in frequency affect the gate bias voltage and hence the 2DEG carrier density (Eqn. C4) whereas in the MESFET, the carrier density in the channel remains the same regardless of changes in frequency. At low frequencies, the 2DEG carrier density is somewhat higher than at high frequencies with a corresponding slight decrease in nonlinearity, giving rise to the decrease in intercept point with increasing frequency. Figure 19 shows an IP2 comparison for the HFET and MESFET switches for identical insertion loss values. The GaAs MESFET switch has slightly better low frequency performance, improving further at frequencies above the gate bias circuit cutoff frequency.

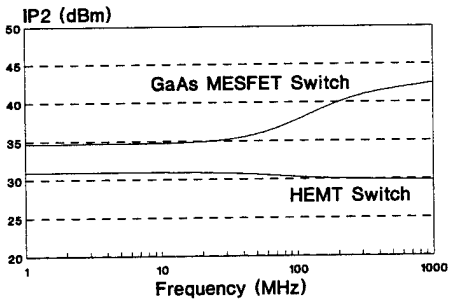

Figure 19. Comparison of the second order distortion intercept point IP2 for the GaN HFET and GaAs MESFET series connected switch in the on-state.

Large Signal Modeling of the AlGaN/GaN FET Microwave and RF Switch

The microwave and RF resistance and capacitance of the AlGaN/GaN HFET will be a function of not only the gate-source voltage but also the source-drain voltage. The capacitive coupling due to the gate capacitances will couple small amounts of RF energy off of the drain and change the original HFET operating conditions. This changing region of operation will heavily influence the operation of these devices in high power microwave and RF control applications. This section presents our first look into the large signal effects (primarily large source-drain voltages) on the microwave and RF resistance and capacitance of the HFET.

In our study, the saturation drain-source DC voltage is assumed to be the same as the small signal model:

$$V_{sd}^{sat} = V_g - V_T, \tag{1}$$

The 2DEG sheet density modulation is known to be a function of both gate-source and source-drain voltage V_{sd} and may be written as:

$$n_s^{'high} = 2n_0 \ln\left(1+\frac{1}{2}\exp\left(\frac{V_g - V_T + \delta V_{sd}}{\eta V_{th}}\right)\right), \quad V_{sd} = MIN\{V_{sd}, V_{sd}^{sat}\} \tag{2}$$

where, V_g is the DC gate voltage, η is the ideality factor, V_{sd} is the source-drain voltage, V_{th} is the thermal voltage for 300 K, V_T is the threshold voltage, and δ is characteristic parameter for the2DEG density ($\delta = 0.05...0.2$).

The expression used for the 2DEG sheet density in the presence of n_{max} is identical to that of the small signal model:

$$n_s^{high} = \frac{n_s^{'high}}{\left(1+\left(n_s^{'high}/n_{max}\right)^{\gamma_1}\right)^{1/\gamma_1}}, \tag{3}$$

The effect of the lateral electric field on the carrier velocity [30] in the heterointerface leads to the following simple equation for large-signal mobility:

$$\mu^{high} = \frac{\mu_n}{\left(1+\frac{\mu_n V_{sd}}{L_{ch}\upsilon_{sat}}\right)^{\gamma_4}}, \quad V_{sd} = MIN\{V_{sd}, V_{sd}^{sat}\}. \tag{4}$$

where, μ_n is the low-field mobility, L_{ch} is the channel length (distance between drain and source regions), υ_{sat} is the saturation velocity in the heterointerface, $\upsilon_{sat} = 3\times10^5$ m/s, V_{sd} is the source-drain voltage

applied between source and drain, and γ_4 is a characteristic parameter for drift velocity, $\gamma_4 = 1 \ldots 2$. This form for the mobility is identical to that of the distortion model presented in a previous section of this report.

Source-drain Resistance

The source-drain resistance R_{sd}^{high} is a function of the parasitic source and drain resistances and the channel resistance which may be written as:

$$R_{sd}^{high} = R_s + R_d + R_{ch}^{'high}, \tag{5}$$

where, the value of the source and drain region resistors R_s and R_d for the symmetrical transistor was written as for the small-signal model as:

$$R_s = R_d = \frac{1}{\mu_{n^+} N_d q} \times \frac{L_{s(d)}}{W h_{n^+}}, \tag{6}$$

where, μ_{n+} is the low-field mobility in 2DEG region not under the gate influence, N_d is electron concentration in the channel region, q is the electronic charge, W is the gate width of HFET, h_{n+} is the depth or thickness of the 2DEG, and $L_{s(d)}$ is the source (or drain) length. Resistor $R_{ch}^{'high}$ represents the source-drain resistance or channel resistance in both conducting and non-conducting states. It is computed as:

$$R_{ch}^{'high} = \frac{R_{ch}^{high}}{\left(1 + \left(R_{ch}^{high} / R_{\max}\right)^{\gamma_2}\right)^{1/\gamma_2}}, \tag{7}$$

where R_{ch}^{high} is related to heterointerface resistance. The two-dimensional gas governs the resistance in this region and the resistance $R_{ch}^{'high}$ may be written as:

$$R_{ch}^{high} = \frac{1}{q n_S^{high} \mu^{high}} \times \frac{L_{ch}}{W}, \tag{8}$$

where μ^{high} is the high-field electron mobility including the effect of the lateral field, n_s^{high} is the sheet density of 2DEG which includes the V_{sd} voltage dependence, and the other symbols have been previously defined.

The resistance R_{max} models the resistance of the bulk GaN:

$$R_{\max} = \frac{1}{q \mu_{GaN} N_{GaN}} \times \frac{L_{ch}}{W h_{GaN}}, \tag{9}$$

where, h_{GaN} is the GaN thickness, N_{GaN} is the GaN electron concentration, and μ_{GaN} is the mobility in GaN. This resistance is extremely large in the typical AlGaN/GaN HFET.

Capacitance C_{sd} and gate-inner side capacitance C_{ig}^{high}.

The influence of n_s^{high} on the gate capacitance is again dependent on the carrier concentration of the 2DEG layer separated by the spacer layer:

$$C_g^{high} = \frac{C_i}{1+2\exp\left(-\frac{V_g - V_T + \delta V_{sd}}{\eta V_{th}}\right)}, \quad V_{sd} = MIN\{V_{sd}, V_{sd}^{sat}\} \tag{10}$$

where, $C_i = \frac{WL\varepsilon_i}{d_i + \Delta d}$. Note the same dependence on the source-drain voltage for the sheet carrier density, which was not considered in the small signal model. Using the same analysis as the small-signal model but including the source-drain voltage parameter, the final relationship for the channel capacitance is:

$$C_g^{high'} = \frac{C_g^{high}}{\left(1+(n_s^{high}/n_{\max})^{\gamma_1}\right)^{1+1/\gamma_1}}. \tag{11}$$

Also, the transaction area for the capacitance reflects the coupling between the gate and the inner side of the source or drain terminals and is a function of V_{sd}:

$$C_{ig}^{high} = C_{ig} \times \left(1-(n_s^{high}/n_{\max})^{\gamma_3}\right)^{1/\gamma_3}, \tag{12}$$

where, $C_{ig} = \frac{\varepsilon_i W}{\pi} \times \ln\left(1+\frac{h_{n^+}}{d_i}\right)$.

Modeling and Measurement Results of High Power Effects

The microwave and RF resistance and capacitance of the AlGaN/GaN HFET will be a function of not only the gate-source voltage but also the source-drain voltage. The capacitive coupling due to the gate capacitances will couple small amounts of RF energy off of the drain and change the original HFET operating conditions. This changing region of operation will heavily influence the operation of these devices in high power microwave and RF control applications. This section presents our first look into the large signal effects (primarily large source-drain voltages) on the microwave and RF resistance and capacitance of the HFET.

The expressions derived in the previous section were used for a first look at the affect of large source-drain voltage on the GaN HFETs. Using these relationships, Figure 20 shows calculated resistance as a function of gate bias and source-drain voltages. Note that for small V_{sd} the resistance is constant for a given gate voltage. As V_{sd} increases beyond approximately 0.25 volts, the resistance gradually increases, increasing this rate for source-drain voltages greater than approximately 1.0 volt. The decrease rate is smaller for zero gate bias voltage.

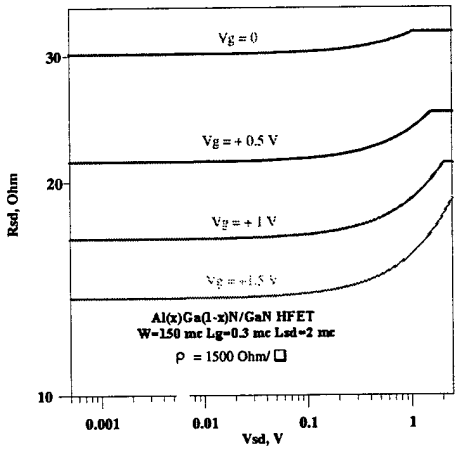

Figure 20. The on-state microwave and RF resistance of the AlGaN/GaN HFET increases substantially above 0.5 volts peak RF voltage. The increase is more dramatic for the positive gate voltages.

Over the same range of voltages the capacitance decreases with increasing source-drain voltage (Figure 21).

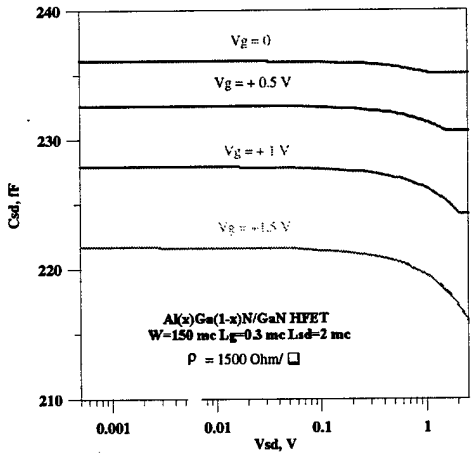

Figure 21. The microwave and RF capacitance of the HFET is relatively constant up to approximately 0.5 volts drain-source peak voltage. The capacitance shows a noticeable decrease with increasing source-drain voltage.

A series of measurements of AlGaN/GaN HFET on-state resistance versus power level were performed over the frequency range of 500 MHz to 8000 MHz using the HP-8510B Vector Network Analyzer. The power level across the shunt HFET was varied from -5 to 20 dBm, which translates into a drain-source voltage level of 0.25 volts peak to 2.25 volts peak. The results of the measurements, shown in Figure 22, indicate that the on-state resistance of the HFET remains relatively constant up to approximately 0 dBm and then increases dramatically above 0 dBm. The frequency dependence of the resistance is due to the change in operating point of the device due to added coupling of the RF voltage

across the gate-source due to the corresponding gate-source and gate-drain capacitances. This effect raises concerns about the use of these devices for very high power operation.

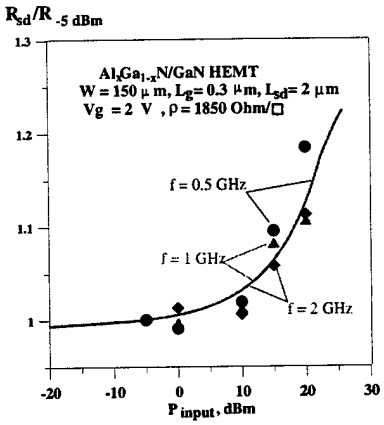

Figure 22. Measured resistance of AlGaN/GaN HEMT control devices as a function of frequency and power level, normalized to the low power (-5 dBm) value. The HFET measured was a 0.3 micron gate length, 150 micron gate width device at +2.0 volts gate voltage.

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Appendix A

2DEG Resistance Model

The two dimensional electron gas (2DEG) governs the resistance in the conducting channel, R_{ch}. The2DEG density n_s is computed with the aid of the following expressions:

$$n_s = 2n_0 \ln\left(1+\frac{1}{2}\exp\left(\frac{V_g - V_T}{\eta V_{th}}\right)\right), \tag{A1}$$

where, V_g is the DC gate voltage, η is the ideality factor, V_{th} is the thermal voltage for 300 K, and V_T is the threshold voltage,

$$n_0 = \frac{\varepsilon_i \eta V_{th}}{2q(d_i + \Delta d)}, \tag{A2}$$

where, ε_i is the dielectric permittivity of $Al_XGa_{1-X}N$ layer, d_I is the thickness of this layer, and Δd_I is the effective thickness of 2DEG. The threshold voltage V_T was calculated for a uniformly doped $Al_XGa_{1-X}N$ layer as [16]:

$$V_T = \Phi_B - \frac{qn_D d_i}{2\varepsilon_i} - \frac{\Delta E_C}{q}, \tag{A3}$$

where, n_D is the surface concentration in $Al_XGa_{1-X}N$, $q\Phi_B$ is the barrier hight between metal gate and $Al_XGa_{1-X}N$, and ΔE_C is the conduction-band discontinuity at the heterojunction. The value of ΔE_C was assumed to be equal to three quarters of the energy gap difference between the $Al_XGa_{1-X}N$ and GaN material. Material parameters of $Al_XGa_{1-X}N$ were determined using linear interpolation between GaN and AlN parameters as a function of the Al molar fraction x [13].

Using the results of Equations A1 through A3, the channel resistance and its gate voltage dependence may be computed as [15]:

$$R_{ch} = \frac{L}{W} \times \frac{1}{\mu_n n_s q}, \tag{A4}$$

where L is the gate length, W is the gate width, q is the single charge, and μ_n is the low-field mobility. The maximum 2DEG carrier density n_{max} in $Al_XGa_{1-X}N$/GaN heterostructure is typically below 1×

10^{13} cm^{-2} [13]. The modified 2DEG carrier density can be written as [17]:

$$n_s' = \frac{n_s}{\left(1+\left(n_s/n_{\max}\right)^{\gamma_1}\right)^{1/\gamma_1}}, \tag{A5}$$

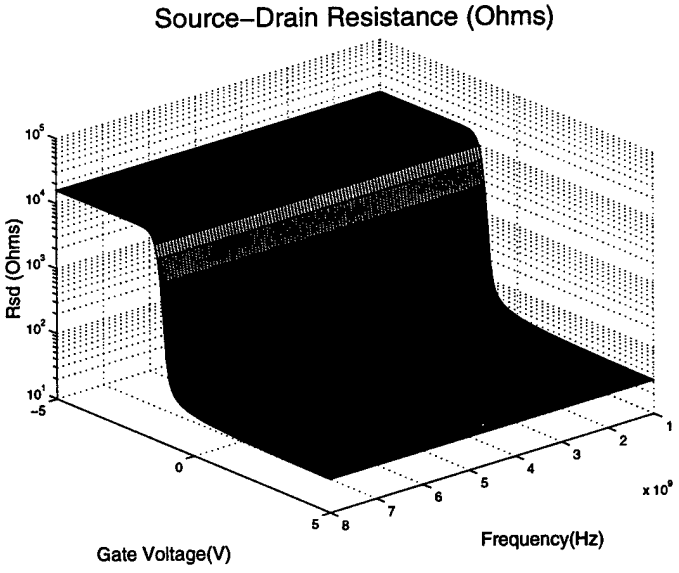
where, γ_1 is the characteristic parameter for the transition to saturation in 2DEG carrier density. Finally Eqn. A5 is substitied into Eqn. 16. Moreover, according to Eqn. A5 the channel resistance grows with n_S decreasing without limit; therefore, in the model, $R_{ch\ max}$ is guaranteed not to exeed several kΩ. Taking all the above factors into account, R_{ch} is written as:

$$R_{ch}' = \frac{R_{ch}}{\left(1+\left(R_{ch}/R_{ch\max}\right)^{\gamma_2}\right)^{1/\gamma_2}}, \tag{A6}$$

where, γ_2 is the characteristic parameter for the transition to reaching the $R_{ch\ max}$.

Using sample parameters as shown in Appendix D, the source-drain resistance was computed as a function of frequency. Figure A1 shows the microwave and RF switching resistance from source to drain in a typical AlGaN/GaN HFET. Note that the source-drain microwave and RF switch resistance of the AlGaN/GaN HFET is relatively constant for a given gate voltage but varies rapidly with gate voltages near threshold.

Figure A1. The source-drain microwave and RF switch resistance of the AlGaN/GaN HFET is relatively constant for a given gate voltage but varies rapidly with gate voltages near threshold.



Appendix B

Capacitance Modeling Details

The Meyer model [17] (for V_{DS} equal to 0) was used for the gate capacitance C_g calculation:

$$C_g = \frac{C_i}{1 + 2\exp\left(-\frac{V_g - V_T}{\eta V_{th}}\right)}, \tag{B1}$$

where, C_I is the above-threshold channel capacitance.

$$C_i = \frac{WL\varepsilon_i}{d_i + \Delta d}. \tag{B2}$$

Taking into account the effect of the 2DEG carrier density saturation (Eqn. A5), the modified expression for C_g may be written as [15]:

$$C_g' = \frac{C_g}{\left(1 + (n_S / n_{\max})^{\gamma_1}\right)^{1+1/\gamma_1}}. \tag{B3}$$

The Meyer model describes the HFET capacitance behavior correctly only above the threshold voltage [19]. When the HFET is used as a control device, the more important capacitance is the one beyond the threshold voltage, because this capacitance determines microwave switch insertion loss or isolation, depending on HFET connection. This capacitance reflects the coupling between the gate and the inner side of the n^+ diffusion regions. To estimate this capacitance, MOSFET capacitance expressions were used [20] because of strong structure similarities between HFET and MOSFET:

$$C_{ig} = \frac{\varepsilon_i W}{\pi} \times \ln\left(1 + \frac{h_{n^+}}{d_i}\right), \tag{B4}$$

where, h_{n+} is the depth of the n^+ - layer.

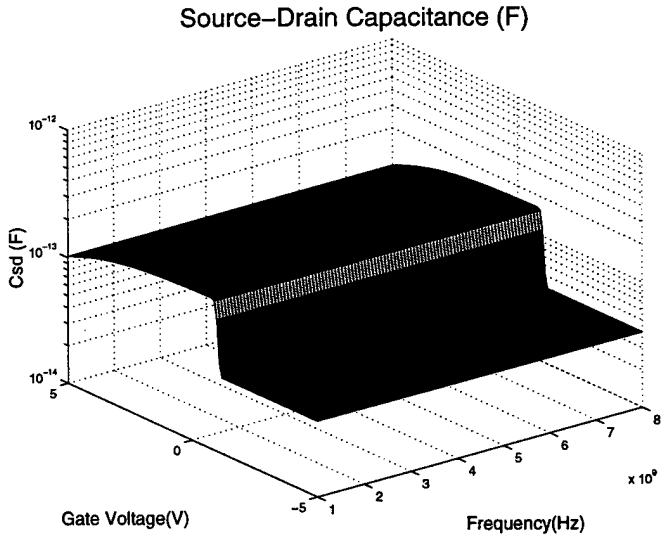
When the 2DEG layer is present this capacitance component (13) is absent, but beyond the threshold voltage V_T , C_{ig} plays the main role. This capacitance appears only after 2DEG suprression. The final approximation for this capacitance may then be written as:

$$C_{ig}' = C_{ig} \times \left(1 - (n_s'/n_{\max})^{\gamma_3}\right)^{1/\gamma_3}, \tag{B5}$$

where, γ_3 is the characteristic parameter for the capacitance C_{ig}. These capacitance terms all contribute to the total off-state capacitance, C_{OFF}. Figure B1 shows the off-state capacitance C_{OFF} as a function of gate bias voltage and frequency. The off-state AlGaN/GaN HFET capacitance is relatively constant with

frequency up to 8.0 GHz but shows a widely varying value near the threshold voltage due to a change-over in the dominant capacitance mechanism. For the test FETs used, the capacitance never exceeds approximately 150 fF.

Figure B1. The off-state AlGaN/GaN HFET capacitance is relatively constant with frequency up to 8.0 GHz but shows a widely varying value near the threshold voltage.



Appendix C

Theoretical Discussion of Distortion in AlGaN/GaN FET Switches

The nonlinear I_{DS}-V_{DS} characteristic for the AlGaN/GaN HFET will govern its production of unwanted distortion products. A general I_{DS}-V_{DS} characteristic for the GaN HFET that includes its nonlinear properties can be written as,

$$I_{DS} = \sum_{n=1}^{\infty} \alpha_n V_{DS}^n \qquad \text{(C1)}$$

where the α_n contain terms dependent on the microwave circuit topology, including such parameters as the gate bias circuitry, gate-drain and gate-source leakage and the device series resistance R_S. A frequently used measure of distortion, the distortion intercept point, is derived for the microwave control element based on this I_{DS}-V_{DS} characteristic. In general applications, the second and third order distortion intercept points (IP2 and IP3, respectively) are of most interest to microwave design engineers and will be discussed here, although higher levels of intercept point may be computed. General expressions for load-referenced IP2 and IP3 can be written for the series reflective GaN HFET-based switch in terms of the expansion parameters in Eqn. C1 [22]. The series reflective switch has been chosen for this discussion since previous studies have shown that in SPDT switch topologies, the series on-state element is the primary distortion generating mechanism [22,23]. With this in mind, the intercept points can be written using the I_{DS}-V_{DS} expansion parameters as [22]:

$$IP2 = \frac{Z_0}{2R_C^4\alpha_2^2}\left(1+\frac{2Z_0}{R_C}\right)^2$$
$$IP3 = \frac{Z_0}{2R_C^3\alpha_3}\left(1+\frac{2Z_0}{R_C}\right) \qquad \text{(C2)}$$

The first order expansion parameter, α_1, is the inverse of the channel series resistance, R_C. Similar intercept point relationships can be derived for more complex switch circuit topologies. The equivalent circuit for the GaN HFET operating in a control mode is shown in Figure C1.

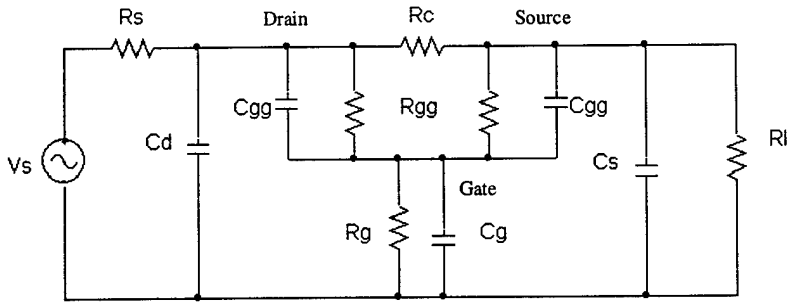


Figure C1. AC equivalent circuit representation for the GaN HFET-based micro wave and RF switch, showing the gate leakage and gate bias equivalent impedances.

The gate bias resistor R_G is used for isolating the gate at all frequencies because of the relatively high impedance of the gate. The resistance R_{GG} represents the gate leakage component. This leakage path is modeled in SPICE as a capacitor-diode parallel circuit; a high value resistor replaces the reverse bias diode in this representation to simplify the analysis.

The electrons in this 2DEG are of very high mobility, and when coupled with the high 2DEG carrier density, a very thin but highly conducting layer is created (Figure C2). The carrier density in this layer can be modulated by the application of a control voltage on the device gate. The I-V characteristics of the GaN HFET are strongly influenced by the field dependent mobility in the 2DEG. High electric fields will occur in the

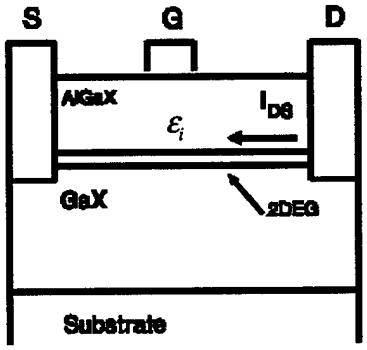


Figure C2. Idealized structure of the a high electron mobility transistor based on an AlGaN/GaN heterostructure. The AlGaN layer is d_i thick; the 2DEG is Δd thick.

conducting channel layer during high power control because of narrow gate lengths, with a corresponding reduction in the channel mobility with increasing voltage drop across the drain-source. A simple model for the velocity-electric field profile is assumed, and the expression for the mobility is derived from the derivative of this profile [3]:

$$v(E) = \frac{\mu_{LF} E}{1 + \frac{\mu_{LF} E}{v_{sat}}}; \mu(E) = \frac{\partial v(E)}{\partial E} = \frac{\mu_{LF}}{[1 + \frac{\mu_{LF} E}{v_{sat}}]^2} \qquad \text{(C3)}$$

where μ_{LF} is the low field mobility, E is the electric longitudinal field in the channel and v_{sat} is the saturation velocity in the 2DEG. Figure C3 shows the model velocity-electric field profile for the a typical heterostructure system.

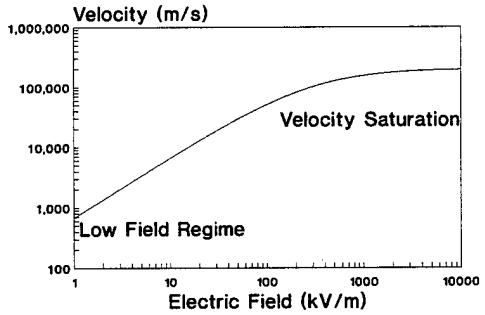


Figure C3. Plot of the velocity-electric field model (Eqn. C3) for a AlGaN/GaN 2DEG..

Typical values for the low field mobility and velocity saturation value in AlGaN/GaN systems are a 0.18 cm^2/V-s and 2.5 x 10^5 m/s, respectively [4,5]. In the 2DEG, a simple approximation for the electric field is V_{DS}/L [3]; this approximation yields a mobility relation versus channel voltage of form:

$$\mu(V) = \frac{\mu_{LF}}{[1 + \frac{\mu_{LF} V}{L v_{sat}}]^2} = \sum_{n=0}^{\infty} \mu_n V^n \quad , \qquad \text{(C4)}$$

The I-V characteristic for the GaN HFET is derived in a similar fashion as the MOSFET [6]; however, the carrier density in the 2DEG above threshold is a function of the capacitance per unit area of the gate-2DEG structure and the gate-source voltage [6]:

$$n_{2DEG} = \frac{\varepsilon_i}{q(d_i + \Delta d)}(V_{GS} - V_{Off}) \tag{C5}$$

By assuming a linear variation of voltage in the channel (similar to MOS square law theory [6]) and the mobility relation in Eqn C3., the nonlinear drain-source current can be written as:

$$I_{DS} = \frac{W}{L}\frac{\varepsilon_i}{d_i + \Delta d}\mu_{LF}\sum_{n=0}^{\infty}\frac{\mu_n}{\mu_0}V_{DS}^{n+1}\left[\frac{V_{GS} - V_{Off}}{n+1} - \frac{V_{DS}}{n+2}\right] \tag{C6}$$

where $\mu_{LF}=\mu_0$. Assuming low field conditions (n=0), the drain current saturates at current I_{Sat}, which occurs at an approximate value of V_{DS} of (V_{GS}-V_{off}). The gate-source voltage in Eqn. C5 is composed of two terms: the dc control component (V_{GS0}) and an ac component as seen in the ac equivalent circuit (Figure C1).

The gate bias and leakage circuits cause the gate voltage to be frequency dependent, causing the ac operating point of the GaN HFET to vary with frequency. The effects of the gate bias circuitry manifest themselves through the gate RC time constant, which is composed of a gate bias resistor R_G , the gate leakage resistance R_{GG}, and the two gate capacitors, C_{GS} and C_{GD}. At low frequencies, the gate impedances are very high, causing the gate to effectively float. At high frequencies, however, the gate-source voltage follows the drain-source voltage due to coupling through C_{GS} and C_{GD}, with the gate being referenced above ground through the gate bias resistance R_G. The relationship between v_{GS} and v_{DS} can be written from the ac equivalent circuit representation of Figure C1 as

$$\gamma = -\frac{v_{GS}}{v_{DS}} = \frac{\frac{Z_S Z_1}{R_C} - Z_G}{Z_1 + Z_S + 2Z_G}, \tag{C7}$$

where $Z_S=1/j\omega C_S$, and Z_1 is the parallel combination of R_{GG} and C_{GS} and C_{GD}. The capacitances C_S and C_D are assumed equal in this result.

From Eqns. C5 and C6, the ac component of the drain-source current relationship can be written strictly as a function of the ac drain-source voltage and the devices operating characteristics:

$$i_{DS} = \frac{2I_{DSat}}{V_{Off}^2}\sum_{n=0}^{\infty}\frac{\mu_n}{\mu_0}v_{DS}^{n+1}\left[\frac{V_{GS0} - V_{Off} - \gamma v_{DS}}{n+1} - \frac{v_{DS}}{n+2}\right] \tag{C8}$$

where I_{DSat} is the drain-source current i_{DS} at saturation for V_{GS0} equal zero. Eqn. C7 provides the means for deriving the expansion coefficients α_n , yielding the distortion parameters of the GaN HFET.

Expanding Eqn. C7 in powers of v_{DS} and grouping terms, the first three expansion coefficients may be written as:

$$\begin{aligned}
\alpha_1 &= \frac{2I_{DSat}}{V_{Off}} = \frac{1}{R_C}, \\
\alpha_2 &= \frac{2I_{DSat}}{V_{Off}}\left(0.5\frac{\mu_1}{\mu_{LF}} - \frac{0.5+\gamma}{V_{Off}}\right), \\
\alpha_3 &= \frac{2I_{DSat}}{V_{Off}}\left(\frac{1}{3}\frac{\mu_2}{\mu_{LF}} - \frac{\mu_1}{\mu_{LF}}\frac{0.5\gamma+(1/3)}{V_{Off}}\right),
\end{aligned} \qquad \text{(C9)}$$

where μ_n (n=1,2) is the mobility expansion coefficient from Eqn. C4.

Appendix D

Typical Values of Simulation Parameters

QUANTITY	SYMBOL IN PROGRAM	UNITS	VALUE
gate width	W	micron	150
gate length	L	micron	0.3
$Al_xGa_{1-x}N$ layer thickness	dins	angstrom	150
2DEG layer thickness	dgas	angstrom	45
Al molar fraction in $Al_xGa_{1-x}N$	mx	-	0.274
Intentional or non-intentional doping in $Al_xGa_{1-x}N$	Ndbulk	cm^{-3}	6×10^{18}
distance between source and drain n^+ regions	Lch	micron	2
distance between source metal and drain metal	Lsd	micron	2
length of source metallization	Ls	micron	25
length of drain metallization	Ld	micron	25
doping of source n+ region,	Nsource	cm^{-3}	1×10^{20}
doping of drain n+ region,	Ndrain	cm^{-3}	1×10^{20}
depth of the n^+ layers	hnlayer	micron	3
thickness of the GaN layer	hGaN	micron	2.716
Intentional or non-intentional doping in GaN	nGaN	cm^{-3}	1×10^{13}
maximal sheet electron concentration in 2DEG	nchmax	m^{-2}	2×10^{17}
measured sheet electron concentration in 2DEG (V_g=0)	nchVg	m^{-2}	0.62×10^{17}
minimum sheet electron concentration in 2DEG (to avoid PC overflow)	nchmin	m^{-2}	1×10^{-1}
permittivity in GaN	epsi	F/m	7.97×10^{-11}
permittivity in sapphire	epssap	F/m	8.8×10^{-11}
low-power electron mobility in heterostructure	mun	$m^2/(V\times s)$	0.0545
low-power electron mobility in GaN	munGaN	$m^2/(V\times s)$	0.0545
subthreshold ideality factor	eta	-	1.5
barrier hight between gate and $Al_xGa_{1-x}N$	Fib	V	0.8
temperature	T	K	300
characteristic parameter for transition to saturation in n_{ch}	gamma1	-	3
characteristic parameter for transition to R_{max}	gamma2	-	0.3
characteristic parameter for transition . to C_{sd} beyond threshold voltage	gamma3	-	1.25
frequency	f	GHz	2.5
characteristic impedance	Zc	Ohm	50
DC gate voltage	Vg	V	-3...+3